



LIST OF PRIOR ART CITED BY  
APPLICANT  
(PTO-1449)

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INTEL-0022

APPLN. SERIAL NO.  
~~New U.S. Patent Application~~ 12/608,423

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June 30, 2003

GROUP  
~~2421~~ 2825

## U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	*PATENT NO.	*ISSUE DATE	*INVENTOR NAME	CLASS	SUBCLASS	FILING DATE

## U.S. PATENT APPLICATION PUBLICATIONS

	*PATENT APPLN. PUB. NO.	*PUB. DATE	*APPLICANT	CLASS	SUBCLASS	

## U.S. PATENT APPLICATIONS

	*APPLN. NO.	*FILING DATE	*INVENTOR	CLASS	SUBCLASS	

## FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No

*PC* Bischoff et al., "Formal Implementation Verification of the Bus Interface Unit for the Alpha 21264 microprocessor", Proc. of 1997 IEEE International Conference on Computer Design: VLSI in Computers and Processors, 12 Oct. 1997, pp. 16-24.

## OTHER ART (Including Author, Title, Date, Pertinent Pages, Publisher, Place of Publication, Etc.)

*P1* Matthew W. Maskewicz, Conor F. Madigan, Ying Zhao, Lintao Zhang, Sharad Malik; Chaff: Engineering an Efficient SAT Solver; June 2001, 530-535; DAC, Las Vegas, Nevada, USA

*P2* R.K. Ranjan, V. Singhal, F. Somenzi, and R.K. Brayton. Using combinational verification for sequential circuits, in: Proc. of Design, Automation and Test in Europe Conference, DATE'99, 1999, pp. 138-144.

*P3* Gabriel P. Bischoff, Karl S. Brace, Samir Jain, and Rahul Razdan; Digital equipment Corporation, Digital Semiconductor, 1997, 16-24, IEEE, Hudson, MA 01749.

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*P5* Z. Khasidashvili, J. Moondanos, Z. Hanna. TRANS: Efficient Sequential Verification of Loop-Free Circuits. in: Proc. of IEEE International High Level Design Validation and Test Workshop, HLDVT02, IEEE Computer Society Press, 2002, p. 115-120, 27-29 Oct. 2002.

EXAMINER

*Phallaka Kike*

DATE CONSIDERED

*9/30/05*

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.